

Application No.: 10/605,571

Docket No.: 22040-00020-US

**AMENDMENTS TO THE CLAIMS**

1. (Currently amended) A multistaged amplification circuit comprising:

a differential amplification circuit, equipped with n differential amplifiers that are connected in a multistaged manner and that amplify and output an input signal from a previous stage to a following stage;

a plurality of transistors connected to said n differential amplifiers that are connected in a multistaged manner, and connected to one constant current source by a current mirror; and

wherein said plurality of transistors are ~~arranged collectively on the side of~~ arranged near said constant current source.

2. (Original) The multistaged amplification circuit according to claim 1, wherein said constant current source is arranged on either an input side or an output side of said differential amplification circuit.

3. (Original) The multistaged amplification circuit according to claim 1, wherein said constant current source is arranged almost in the center of said n differential amplifiers connected in a multistaged manner.

4. (Currently amended) The multistaged amplification circuit according to claim 1, wherein said plurality of transistors are collectively grounded to the same place via separate ground lines.

5. (Currently amended) A multistaged amplification circuit, comprising:

a differential amplification circuit, equipped with n differential amplifiers that amplify and output an input signal from a previous stage to a following stage, and that are connected in a multistaged manner;

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a plurality of transistors connected to a plurality of differential amplifiers and one constant current by a current mirror for every group into which said n plurality of differential amplifiers are divided; and

wherein said plurality of transistors are ~~arranged collectively on the side of~~ arranged near said constant current source for every said group.

6. (Currently amended) A multistaged amplification circuit comprising:

a differential amplification circuit, equipped with n differential amplifiers that amplify and output an input signal from a previous stage to a following stage, and that are connected in a multistaged manner;

a plurality of transistors connected to said n differential amplifiers that are connected in a multistaged manner, and that are connected to one constant current source by a current mirror; and

wherein said plurality of transistors are collectively grounded to the same place via separate ground lines.

7. (New) A multistaged amplification circuit comprising:

a differential amplification circuit, equipped with n differential amplifiers that are connected in a multistaged manner and that amplify and output an input signal from a previous stage to a following stage;

a plurality of transistors connected to said n differential amplifiers that are connected in a multistaged manner, and connected to one constant current source by a current mirror; and

a plurality of separate ground lines,

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wherein each of said plurality of transistors is connected to a common ground node by a dedicated one of the plurality of separate ground lines.

8. (New) The multistaged amplification circuit of claim 7, wherein the plurality of separate ground lines collectively suppress a distributed voltage drop.

9. (New) A multistaged amplification circuit, comprising:

a differential amplification circuit, equipped with n differential amplifiers that amplify and output an input signal from a previous stage to a following stage, and that are connected in a multistaged manner;

a plurality of transistors connected to a plurality of differential amplifiers and one constant current by a current mirror for every group into which said n plurality of differential amplifiers are divided; and

means for suppressing a ground line distributed voltage drop associated with each of the plurality of transistors.

10. (New) The multistaged amplification circuit of claim 9, wherein the means for suppressing a ground line distributed voltage drop reduces electrical noise.

11. (New) The multistaged amplification circuit of claim 9, wherein the means for suppressing a ground line distributed voltage drop preserves linearity of an amplified signal.

12. (New) The multistaged amplification circuit of claim 9, wherein the means for suppressing a ground line distributed voltage drop stabilizes a high frequency operating characteristic of the multistaged amplification circuit.

13. (New) The multistaged amplification circuit of claim 9, wherein the means for suppressing a ground line distributed voltage drop reduces electrical

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noise, preserves linearity of an amplified signal, and stabilizes a high frequency operating characteristic of the multistaged amplification circuit.

14. (New) The multistaged amplification circuit of claim 9, wherein the means for suppressing a distributed voltage drop comprises a plurality of separate ground lines,

wherein each of said plurality of transistors is connected to a common ground node by a dedicated one of the plurality of separate ground lines.